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EXAMINER	
ORTIZ CRIADO, JORGE L	
ART UNIT	**PAPER NUMBER**
2656	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,244	KIYOSE, MASASHI	
	Examiner	Art Unit	
	Jorge L. Ortiz-Criado	2656	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,10,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6, 10, 12 and 13* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413). Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 2, 3, 4, 10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graham et al. U.S. Patent no. 5,072,195 in view of Shigemori U.S. patent No. 6,693,862.

Regarding claim 2, Graham et al. discloses a "PLL"/(phase locked loop) circuit comprising:

a first loop circuit for generating a first clock signal which is synchronized with a first reference signal (wide/broad range of frequencies), wherein the first reference signal is compared with the first clock signal to generate a first control voltage (See Fig. 5, ref# 500a, 5001a, 502a, 503a; col. 7, lines 7-53); and

a second loop circuit connected to the first loop circuit for generating a second clock signal which is synchronized with a second reference signal having a frequency which is sufficiently lower than the frequency of the first reference signal (narrow range, target frequency within the wide/broad range of frequencies having a maximum and minimum frequencies within

the range), wherein the second reference signal is compared with the second clock signal to generate a second control voltage (See Fig. 5, ref# 500b, 5001b, 502b, 503b; col. 7, lines 7-53; see col. 8, line 66 to col. 9, line11);

wherein the first loop circuit includes a first voltage controlled oscillator for generating the first clock signal in accordance with the first control voltage (See Fig. 5, ref# 503a-VCO1, "Va"); and

wherein the second loop circuit includes a second voltage controlled oscillator for generating the second clock signal in accordance with the first control voltage and the second control voltage (See Fig. 5, ref# 503b-VCO2, "Va, Vb").

Graham et al. does not expressly disclose wherein the first reference signal is a wobble signal of an optical disc, and specifically the second reference signal is a land prepit signal of the optical disc.

However, this is well known in the art and is evidenced by Shigemori, which teaches using a PLL circuit having a first reference signal as a wobble signal of an optical disc, and a second reference signal is a land prepit signal of the optical disc (see Fig. 1 ref# 18)

It would have been obvious to one with an ordinary skill in the art at the time of the invention to provide the a first reference signal as a wobble signal of an optical disc, and a second reference signal is a land prepit signal of the optical disc, in order to make the PLL circuit being implemented for generating a clock for a data recording system, as taught by Shigemori.

Regarding claim 3 and 10, Graham et al. in combination with Shigemori shows wherein the second loop circuit further includes an adder connected to the second voltage controlled

oscillator for generating a sum voltage by adding the first control voltage and the second control voltage (See Graham et al. col. 7, lines 54-63, Fig. 5, ref#520, signal Vab =Va + Vb)

Regarding claim 4, Graham et al. discloses "PLL"/(phase locked loop) circuit comprising:

a first loop circuit for generating a first clock signal which is synchronized with a first reference signal; and a second loop circuit connected to the first loop circuit for generating a second clock signal which is synchronized with a second reference signal, wherein the frequency of the second reference signal is lower than the frequency of the first reference signal; wherein the first loop circuit includes (See Fig. 5, ref# 500a, 5001a, 502a, 503a; col. 7, lines 7-53);(See Fig. 5, ref# 500b, 5001b, 502b, 503b; see col. 8, line 66 to col. 9, line11) (narrow range, target frequency within the wide/broad range of frequencies having a maximum and minimum frequency within the range):

a first frequency divider for generating a first divisional clock signal by dividing the first clock signal by a predetermined first frequency dividing ratio (See Fig. 5, ref# 504a);

a first phase comparator connected to the first frequency divider for receiving the first reference signal and the first divisional clock signal and generating a first comparison signal in accordance with the first reference signal and the first divisional clock signal (See Fig. 5, ref# 501a);

a first low-pass filter connected to the first phase comparator for generating a first control voltage corresponding to the first comparison signal (See Fig. 5, ref# 502a); and

a first voltage controlled oscillator connected to the first low-pass filter for generating the first clock signal in accordance with the first control voltage(See Fig. 5, ref# 503a);

wherein the second loop includes:

a second frequency divider for generating a second divisional clock signal by dividing the second clock signal by a predetermined second frequency dividing ratio (See Fig. 5, ref# 504b);

a second phase comparator connected to the second frequency divider for receiving the second reference signal and the second divisional clock signal and generating a second comparison signal in accordance with the second reference signal and the second divisional clock signal (See Fig. 5, ref# 501b);

a second low-pass filter connected to the second phase comparator for generating a second control voltage corresponding to the second comparison signal (See Fig. 5, ref# 502b); and

a second voltage controlled oscillator connected to the first and second low-pass filters for generating the second clock signal in accordance with the first and second control voltages (See Fig. 5, ref# 503b).

Graham et al. does not expressly disclose wherein the first reference signal is a wobble signal of an optical disc, and specifically the second reference signal is a land prepit signal of the optical disc.

However, this is well known in the art and is evidenced by Shigemori, which teaches using a PLL circuit having a first reference signal as a wobble signal of an optical disc, and a second reference signal is a land prepit signal of the optical disc (see Fig. 1 ref# 18)

It would have been obvious to one with an ordinary skill in the art at the time of the invention to provide the a first reference signal as a wobble signal of an optical disc, and a second reference signal is a land prepit signal of the optical disc, in order to make the PLL circuit being implemented for generating a clock for a data recording system, as taught by Shigemori.

Regarding claim 12 and 13, method claims 12 and 13 are drawn to the corresponding method of the apparatus as claimed in claims 2 and 3. Therefore method claims 12 and 13 correspond to apparatus claims 2 and 3, and are rejected for the same reasons of obviousness as used above.

2. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Graham et al. U.S. Patent no. 5,072,195 in combination with Shigemori U.S. patent No. 6,693,862 and further in view of Lee et al. U.S. Patent No. 5,734,301.

Graham et al. in combination with Shigemori teaches a second voltage controlled oscillator connected to the first and second low-pass filters for generating the second clock signal in accordance with the first and second control voltages, but does not expressly disclose wherein the second voltage controlled oscillator includes: a first input terminal for receiving the first control voltage; a second input terminal for receiving the second control voltage; and a ring oscillator connected to the first and second input terminals and driven by differing first and second control currents respectively corresponding to the first and second control voltages.

However this feature is well known in the art as evidenced by Lee et al. which discloses a PLL circuit comprising a first loop circuit for generating a first clock signal which is

synchronized with a first reference signal; and a second loop circuit connected to the first loop circuit for generating a second clock signal which is synchronized with a second reference signal, a first voltage controlled oscillator connected to a first low-pass filter for generating the first clock signal in accordance with the first control voltage, a second voltage controlled oscillator connected to the first and second low-pass filters for generating the second clock signal in accordance with the first and second control voltages (See col. 1, line 63 to col. 2, line 4; col. 2, line 51 to col. 3 line 47; Fig. 1),

wherein the second voltage controlled oscillator includes: a first input terminal for receiving the first control voltage; a second input terminal for receiving the second control voltage; and a ring oscillator connected to the first and second input terminals and driven by differing first and second control currents respectively corresponding to the first and second control voltages (See col. 5, line 63 to col. 6, line 19; Fig. 6)

Therefore it would have been obvious to one with an ordinary skill in the art at the time of the invention to include voltage controlled oscillator that includes a first input terminal for receiving the first control voltage; a second input terminal for receiving the second control voltage and a ring oscillator connected to the first and second input terminals and driven by differing first and second control currents respectively corresponding to the first and second control voltage, as taught by Lee et al., in order to provide broadband/coarse control/tuning and narrow/fine control/tuning to the voltage control oscillator.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Graham et al. U.S. Patent no. 5,072,195 in combination with Shigemori U.S. patent No. 6,693,862 and Lee et al. U.S. Patent No. 5,734,301, and further in view of Yoshizawa U.S. patent No. 5,909,474.

Graham et al. in combination with Shigemori and Lee et al. teaches wherein the second voltage controlled oscillator further includes: a first current control gate corresponding to the first input terminal; and a second current control gate corresponding to the second input terminal; wherein a drive current of the first current control gate is greater than a drive current of the second current control gate (See Lee et al. col. 5, line 63 to col. 6, line 19; Fig. 6); and wherein the first voltage controlled oscillator includes a third input terminal for receiving the first control voltage (See Lee et al. Figs. 1,3) ;

But does not expressly teaches a fourth input terminal for receiving a constant DC voltage.

However this feature is well known in the art as evidenced by Yoshizawa, which discloses a PLL circuit comprising a first loop circuit for generating a first clock signal which is synchronized with a first reference signal; and a second loop circuit connected to the first loop circuit for generating a second clock signal which is synchronized with a second reference signal, a first voltage controlled oscillator connected to a first low-pass filter for generating the first clock signal in accordance with the first control voltage, a second voltage controlled oscillator connected to the first and second low-pass filters for generating the second clock signal in accordance with the first and second control voltages wherein the second voltage controlled oscillator includes: a first input terminal for receiving the first control voltage; a second input terminal for receiving the second control voltage; and a ring oscillator connected to the first and

second input terminals and driven by differing first and second control currents respectively corresponding to the first and second control voltages wherein the first voltage controlled oscillator includes a third input terminal for receiving the first control voltage and a fourth input terminal for receiving a constant DC voltage (See col. 3, line 45 to col. 4, line 26; col. 5, line 58 to col. 6, line 5;

Therefore it would have been obvious to one with an ordinary skill in the art at the time of the invention to include the fourth input terminal for receiving a constant DC voltage to be used as a reference constant voltage since the voltage control oscillator is a ring type, as taught by Yoshizawa, in order to provide the coarse/broadband control/tuning in the first oscillator to further eliminating the phase difference between the first reference signal and the clock signal.

Allowable Subject Matter

4. Claim 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 09/15/2005 have been fully considered but they are not persuasive.

Applicants argues that Shigemori does not disclose a first loop for generating a first clock signal which is synchronized with a first reference signal and a second loop for generating a second clock signal which is synchronized with a second reference signal, the first reference signal being a wobble signal of an optical disc and the second reference signal being a land prepit signal of the optical disc, as required in each of independent claims 2,4 and 12. Rather, Shigemori discloses a PLL circuit that generates a clock signal, which synchronized with a wobble signal and prepit signal. Applicant's argument is not persuasive because the rejection was based on Graham in view of Shigemori, not based on Shigemori alone. Shigemori was used for the teaching of a PLL circuit that generates a clock signal, which is synchronized with a wobble signal and prepit signal.

Furthermore, Applicants argues that providing the wobble signal to Graham's reference phase –locked loop 500a, would not accurately reflects the rotation of an optical disc.

Applicant's argument is not persuasive because Graham's discloses where the a first loop 500a generates a first clock signal which is synchronized with a first reference signal; and a second loop circuit connected to the first loop circuit for generating a second clock signal which is synchronized with a second reference signal, wherein the frequency of the second reference signal is lower than the frequency of the first reference signal. As set forth in the rejection, Graham et al does not expressly disclose that the used first reference signal is the wobble signal of an optical disc. However, Graham et al. discloses the PLL structure as claimed, and the provision of the wobble signal to the first loop 500a and the second reference signal as the prepit, would not affect the reference phase-locked loop500a by duty ratio of the binary-coded wobble signal and would accurately reflects the rotation of an optical disc, since Graham et al. discloses

the same PLL structure of Applicant's PLL structure claimed. This is true in view of Shigemori, which is used for the teaching of a PLL circuit that generates a clock signal, which is synchronized with a first reference signal being provided as a wobble signal and a second reference signal being provided as the prepit signal of an optical disc. Hence, it would be understood to one of ordinary skill in the art and hence would be obvious providing a first and second reference signals as being the wobble signal and the prepit signals to obtain the clock signal. The Examiner cannot find a structural difference between the claimed PLL structure invention and the prior art in order to patentably distinguish the claimed invention from the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jorge L. Ortiz-Criado whose telephone number is (571) 272-7624. The examiner can normally be reached on Mon.-Thu.(8:30 am - 6:00 pm),Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa Thi Nguyen can be reached on (571) 272-7579. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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11/28/05